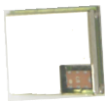
SPK ELECTRONICS CO., LTD.

Bluetooth Module Datasheet

Doc. Version: 20151208



Product ID	**SPK-EBMA17**
Product Name	**Class 2 V2.1+EDR BC04 ROM(A07) module**
Firmware Version	
Hardware Version	**Rev.1.0.5**

1. DESCRIPTION

SPK-EBMA17 is a EEPROM integrated bluetooth class 2 module, using CSR BlueCore4-ROM solution to build in module, the device become bluetooth enabled, and can communicate wirelessly with other bluetooth device in a line-of-sight short range (>10 meters).

SPK-EBMA17 implements the HCI commands for the bluetooth hardware by accessing lower layer stacks commands and registers.

With its sufficient pin definitions, high receiving sensitivity, low power consumption and low cost, SPK-EBMA17 is suitable for numerous electronic devices.

2. FEATURE

- Comply with full qualified bluetooth specification V2.1+EDR(Enhanced Data Rate)
- Build in CSR BC04 ROM(A07)
- Full-speed bluetooth operation with full Piconet support
- Scatternet support
- Low Power Consumption
- Support for 802.11 Co-existence, support 2-wire and 3-wire.
- Support standard HCI (UART, USB) host interface
- Integrated 26MHz Reference Clock
- Integrated 16kbits EEPROM
- RoHS Compliant
- Support V2.1 mandatory functionality

➢➢ Adaptive Frequency Hopping (AFH)

➢➢ Faster connections

- Flow and Flush timeout
- LMP improvements
- Parameter ranges
- Extended SCO (eSCO), eV3 +CRC, eV4, eV5
- Scatter mode
- LMP Absence Masks, Quality of service and SCO handle
- L2CAP flow and error control
- Synchronization

• Mini form factor **7.5 * 6.5 * 1.6mm** and Low Profile using high-density packaging technology for space critical applications.
• RF output power –20dBm ~ +4 dBm (class 2).
• High receiving sensitivity (-83 dBm 0.1%BER).

3. APPLICATIONS

USB dongle, NB, Pocket PC, PDAs, USB/UART adapter, MP3 Player, Cellular Phones, Digital Cameras and other high volume consumer products

4. SPECIFICATIONS

4.1 General Specification

ITEMS	SPECIFICATION
Supply Voltage	VDD: 3.3V+/-0.3V Regulated supply voltage
Carrier Frequency	2402MHz to 2483.5MHz
Modulation Method	GFSK, 1Mbps, 0.5BT Gaussian
Data Rate (MAX) 1M	Asynchronous:723.2kbps/57.6kbps Synchronous:433.9kbps
Data Rate (MAX) 2M	Asynchronous:1448.4kbps/115.2kbps Synchronous:864.7kbps
Data Rate (MAX) 3M	Asynchronous:2178.1kbps/177.1kbps Synchronous:1306.9kbps
Transmission Output Power	+4dBm
Hopping	1600hops/sec, 1MHz channel space
Receiving Signal Range	-83dBm
Receiver IF Frequency	1.5MHz center frequency
Baseband Crystal OSC	26MHz

Output Interface	UART, USB
Operation Temperature	-40℃ to +85℃
Absolute Max Supply Voltage	3.6V for VDD, other VDD +0.3V
Storage Temperature	-40℃ to +150℃
Baking condition	125℃/24hrs or 45℃/192hrs
Scatternet	Support
Bluetooth Specification	V2.1+EDR
Antenna Impedance	50Ω
USB Specification	Ver2.0

4.2. Electrical Characteristics

4.2.1 Transmitter Section

ITMES		Min	Typ	Max	Unit	Condition
Transmission power		-6	+1.5	+4	dBm	Longest supported packet
Initial Frequency Accuracy		-75		75	KHz	Hopping ON/OFF Continuous TX
In-band spurious M +/- 500 kHz |M-N|=2 |M-N|□3 Exception				 -20 -20 -40 -20	 dBc dBm dBm dBm	Max hold and 100kHz
Out of band spurious (Operation mode) 30MHz to 1GHz 1GHz to 12.75GHz 1.8GHz to 1.9GHz 5.1GHz to 5.3GHz				 -36 -30 -47 -47	 dBm dBm dBm dBm	100kHz RBW
Adjacent Channel Power ± 2MHz >± 3MHz				 -20 -40	 dB dB	
Modulation Characteristics	F1AVG	140		175	KHz	00001111,Hopping off DH1
	F2MIN	115			KHz	01010101,Hopping off DH1
	F2AVG/F1AVG	0.8				

Frequency Drift			±25 ±40 ±40	KHz KHz KHz	DH1 DH3 DH5 Max Drift rate:400Hz/10us
Operation current		60		mA	Peak Current during bust
EDR Relative Transmit Power	-4	-2	1	dB	
EDR Max Carrier Frequency Stability					
1) Wo	-10	2	10	KHz	
2) Wi	-75	6	75	KHz	
3) | Wo+Wi |	-75	8	75	KHz	
EDR π/4 DQPSK Modulation Stability					
1) RMS DEVM		7	20	%	
2) 99% DEVM		13	30	%	
3) Peak DEVM		19	35	%	
EDR 8DPSK Modulation Stability					
1) RMS DEVM		7	13	%	
2) 99% DEVM		13	20	%	
3) Peak DEVM		17	25	%	
EDR In-band Spurious Emission					
1) F > Fo + 3MHz		<-50	-40	dBm	
2) F > Fo – 3MHz		<-50	-40	dBm	
3) F = Fo – 3MHz		-46	-40	dBm	
4) F = Fo – 2MHz		-34	-20	dBm	
5) F = Fo – 1MHz		-35	-26	dB	
6) F = Fo + 1MHz		-35	-26	dB	
7) F = Fo + 2MHz		-31	-20	dBm	
8) F = Fo + 3MHz			-40	dBm	
EDR Sensitivity at 0.01% BER					
1) π/4 DQPSK		-83	-70	dBm	
2) 8DPSK		75	-70	dBm	
EDR Maximum received signal at 0.1% BER					
1) π/4 DQPSK		-20	-8	dBm	
2) 8DPSK		-20	-10	dBm	
EDRπ/4 DQPSK C/I Performance					

1) Co-Channel interference at 0.1% BER		10	13	dB	
2) Adjacent (1 MHz) interference		-10	0	dB	
3) Adjacent (2 MHz) interference		-40(-23)	-30(-15)	dB	
4) Adjacent (□3 MHz) interference		-45	-40	dB	
5) Image frequency interference		-20	-7	dB	
EDR 8DPSK C/I Performance					
1) Co-Channel interference at 0.1% BER		19	21	dB	
2) Adjacent (1 MHz) interference		-5	5	dB	
3) Adjacent (2 MHz) interference		-40(-20)	-25(-10)	dB	
4) Adjacent (□3 MHz) interference		-45	-33	dB	
5) Image frequency interference		-15	0	dB	

4.2.2 Receiver Section

ITMES	Min	Typ	Max	Unit	Condition
Sensitivity Single slot packet Multi slot packet	 -83 -83	 -80 -80	 -76 -76	 dBm dBm	BER 10E-3,hopping off/1600K returned payload bit Multi slot packets uses DH5
Maximum received signal	-20	-5		dBm	BER 10E-3, hopping off 1600K returned payload bit, multi slot packet, DH1
Out-band blocking 30MHz to 2000MHz 2000MHz to 2399MHz 2498MHz to 3000MHz 3000MHz to 12.75GHz (idle mode) 30MHz to 1GHz 1GHz to 12.75GHz 1.8GHz to 1.9GHz 5.15GHz to 5.3GHz	 -10 -27 -27 -10		 -57 -47 -47 -47	 dBm dBm dBm dBm dBm dBm dBm dBm	Hopping off,BER 10E-3
Inter modulation N=5	-39			dBm	Hopping off,BER 10E-3
Interference Performance Co-channel Adjacent(1MHz) to In-band image		 8	 11 -16	 dB dB	BER 10E-3 Measured at hopping off.

4.3 Interface

Interface	Description
UART Interface	TX, RX, RTS, CTS(9600bps~1.5Mbps)
SPI Interface	Synchronous Serial Interface for firmware download
USB Interface	Full speed Universal Serial Bus interface
PCM Interface	Supports continuous transmission and reception of PCM encoded audio data over Bluetooth
PIO Interface	8 terminals
AIO Interface	1 terminals

4.4 Current consumption

Operation Mode	Connection Type	UART Rate (kbps)	Average	Unit
Page scan, time interval 1.28s	-	115.2	0.41	mA
Inquiry and page scan	-	115.2	0.77	mA
ACL No traffic	Master	115.2	6.4	mA
ACL With file transfer	Master	115.2	11	mA
ACL No traffic	Slave	115.2	14	mA
ACL With file transfer	Slave	115.2	17	mA
ACL 40ms sniff	Master	38.4	1.5	mA
ACL 1.28s sniff	Master	38.4	0.19	mA
SCO HV1	Master	38.4	34	mA
SCO HV3	Master	38.4	17	mA
SCO HV3 30ms sniff	Master	38.4	17	mA
ACL 40ms sniff	Slave	38.4	1.5	mA
ACL 1.28s sniff	Slave	38.4	0.24	mA
Parked 1.28s beacon	Slave	38.4	0.18	mA
SCO HV1	Slave	38.4	34	mA
SCO HV3	Slave	38.4	21	mA
SCO HV3 30ms sniff	Slave	38.4	17	mA
Standby Host connection (Deep Sleep)	-	38.4	0.03	mA
Reset (RESET low)	-	-	0.04	mA

4.5 External Reference Clock Input

The SPK-EBMA17 RF local oscillator and internal digital clocks are derived from the reference clock at SPK-EBMA17 XTAL_IN input. This reference may be either an external clock or from a crystal connected between XTAL_IN and XTAL_OUT. The external clock can either be a digital level square wave or sinusoidal and this may be directly coupled to XTAL_IN without the need for additional components. If the peaks of the reference clock are below 0 V or above 1.8 V, it must be driven through a DC blocking capacitor (~33pF) connected to XTAL_IN. The external clock signal should meet the specifications as below table.

If the external clock is driven through a DC blocking capacitor then maximum allowable amplitude is reduced from 1.8V to 800mV pk-pk.

	Min	Typ	Max
Frequency	7.5 MHz	26 MHz	40 MHz
Duty cycle	20 : 80	50 : 50	80 : 20
Edge Jitter (At Zero Crossing)	-	-	15ps rms
Signal Level	400mV pk-pk	-	1.8V *

4.6 Host transport selection

Pin Values			Host Transport	Features	
PIO[0]	PIO[1]	PIO[4]		Auto System Clock Adaptation	Auto Baud Rate Adaptation
0	0	0	BCSP (default)	Available (Note 1)	Available (Note 2)
0	0	1	BCSP with UATR configured to use 2 stop bits and no parity	Available (Note 1)	Available (Note 2)
0	1	0	USB, 16 MHz crystal	Not available	Not appropriate
0	1	1	USB, 26 MHz crystal	Not available	Not appropriate
1	0	0	Three-wire UART	Available (Note 1)	Available (Note 2)
1	0	1	H4DS	Available (Note 1)	Available (Note 2)
1	1	0	UART (H4)	Available (Note 1)	Available (Note 2)
1	1	1	Undefined	-	-

The firmware configures itself when it boots by reading the values on a set of PIO pins.

Note 1 : If a UART-based host transport is selected and the firmware does not know its clock frequency (because PSKEY_ANA_FREQ contains no value), then the firmware attempts to lock on to the available system clock signal. Use of this mechanism implies booting the firmware twice, as described in [AUTOBAUD]. PSKEY_ANA_FREQ has no default value.

Note 2 : If a UART-based host transport is selected and the baud rate defined in PSKEY_UART_BAUDRATE is zero (the default value), then the baud rate adaptation process is invoked, as described in [AUTOBAUD].

If the PS Key contains a non-zero baud rate then the UART is configured with this value. If the system clock adaptation mechanism is used, it may result in the processor running slower than normal, so the consequent (measured) baud rate will also be affected.

4.7 Audio PCM Interface

Pulse Code Modulation (PCM) is a standard method used to digitize audio (particularly voice) patterns for transmission over digital communication channels. Through its PCM interface, SPK-EBMA17 has hardware support for continual transmission and reception of PCM data, so reducing processor overhead for wireless headset applications. SPK-EBMA17 offers a bi-directional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.

Hardware on SPK-EBMA17 allows the data to be sent to and received from a SCO connection.

Up to three SCO connections can be supported by the PCM interface at any one time(1). SPK-EBMA17 can operate as the PCM interface Master generating an output clock of 128, 256 or 512kHz. When configured as PCM interface slave it can operate with an input clock up to 2048kHz. eGM-A1 is com7patible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13 or 16-bit linear, 8-bit μ-law or A-law companded sample formats at 8ksamples/s, and can receive and transmit on any selection of three of the first four slots following PCM_SYNC. The PCM configuration options are enabled by setting the PS Key PS KEY_PCM_CONFIG.

eGM-A1 inter7 faces directly to PCM audio devices including the following:

* Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
* OKI MSM7705 four channel A-law and μ-law CODEC
* Motorola MC145481 8-bit A-law and μ-law CODEC
* Motorola MC145483 13-bit linear CODEC
* STW 5093 and 5094 14-bit linear CODECs
* DFBM-CS321 is also compatible with the Motorola SSI. interface

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4.7.1 PCM Interface Master/Slave

When configured as the Master of the PCM interface, SPK-EBMA17 ngenerates PCM_CLK and PCM_SYNC.

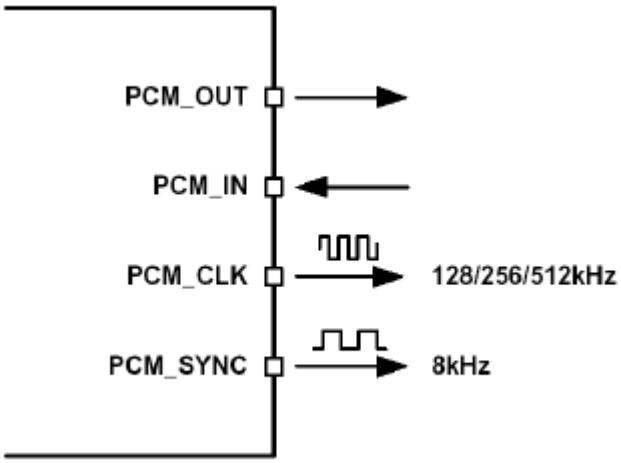


Figure 1: SPK-EBMA17 as PCM Interface Master

When configured as the Slave of the PCM interface, SPK-EBMA17 accepts PCM_CLK rates up to 2048kHz.

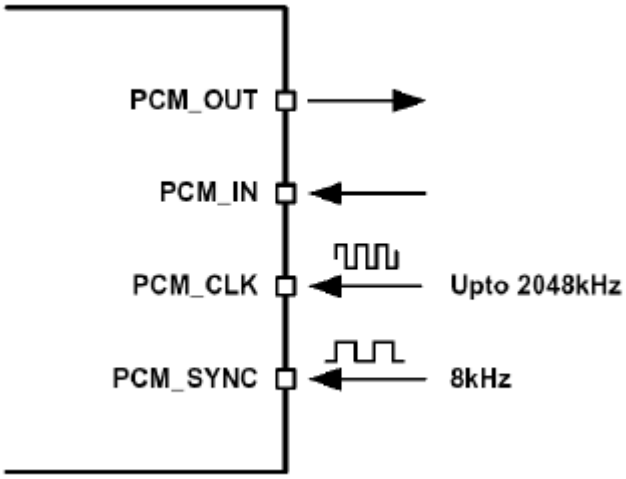


Figure 2: SPK-EBMA17 as PCM Interface Slave

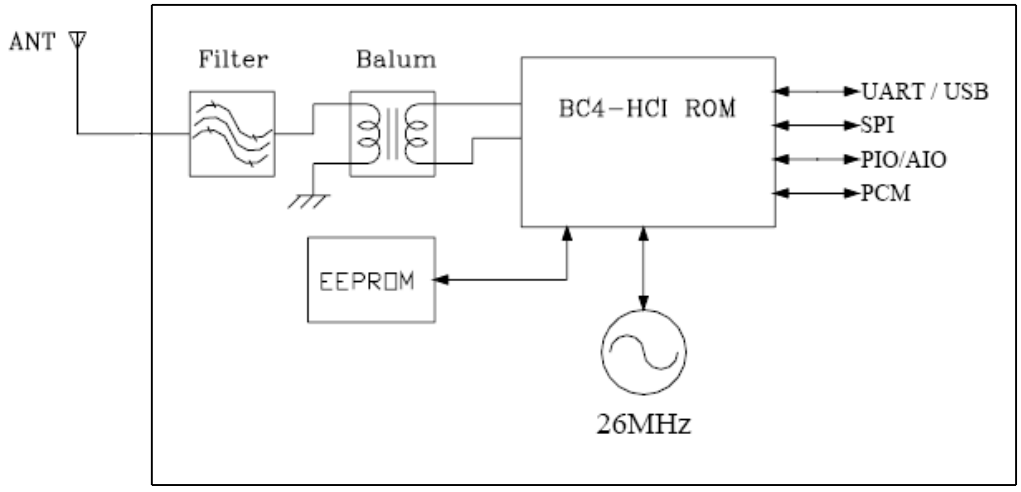
4.7.1.1 PCM Master Timing

Symbol	Parameter	Min	Typ		Max	Unit
fmclk	PCM_CLK frequency	4MHz DDS generation. Selection of frequency is programmable	-		128 256 512	kHz
		48MHz DDS generation. Selection of frequency is programmable	2.9		-	kHz
-	PCM_SYNC frequency		-	8		kHz
tmclkh(1)	PCM_CLK high 4MHz DDS generation		980	-	-	ns
tmclkl(1)	PCM_CLK low 4MHz DDS generation		730	-		ns
-	PCM_CLK jitter 48MHz DDS generation			-	21	ns pk-pk
tdmclksynch	Delay time from PCM_CLK high to PCM_SYNC high		-	-	20	ns
tdmclkpout	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
tdmclklsyncl	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)		-	-	20	ns
tdmclkhsyncl	Delay time from PCM_CLK high to PCM_SYNC low		-	-	20	ns
tdmclklpoutz	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
tdmclkhpoutz	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
tsupinclkl	Set-up time for PCM_IN valid to PCM_CLK low		30	-	-	ns
thpinclkl	Hold time for PCM_CLK low to PCM_IN invalid		10	-	-	ns

4.7.1.2 PCM Slave Timing

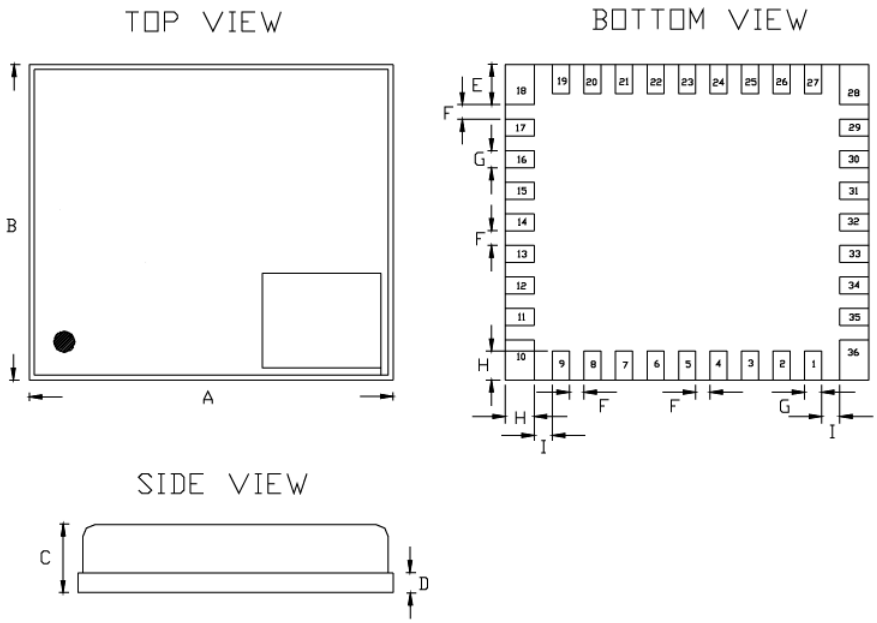
Symbol	Parameter	Min	Typ	Max	Unit
fsclk	PCM clock frequency (Slave mode: input)	64	-	2048	kHz
fsclk	PCM clock frequency (GCI mode)	128	-	4096	kHz
tsclkl	PCM_CLK low time	200	-	-	ns
tsclkh	PCM_CLK high time	200	-	-	ns
thsclksynch	Hold time from PCM_CLK low to PCM_SYNC high	30	-	-	ns
tsusclksynch	Set-up time for PCM_SYNC high to PCM_CLK low	30	-	-	ns
tdpout	Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
tdsclkhpout	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
tdpoutz	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
tsupinsclkl	Set-up time for PCM_IN valid to CLK low	30	-	-	ns
thpinsclkl	Hold time for PCM_CLK low to PCM_IN invalid	30	-		ns

5. BLOCK DIAGRAM



6. PIN CONFIGURATION AND MECHANICAL DIMENSION

6.1 Pin Placement



A	7.5 ± 0.2mm	D	0.4 ± 0.05mm	G	0.35 ± 0.05mm
B	6.5 ± 0.2mm	E	0.825 ± 0.05mm	H	0.6 ± 0.05mm
C	1.6mm max.	F	0.3 ± 0.05mm	I	0.375 ± 0.05mm

6.2 Pin Definition

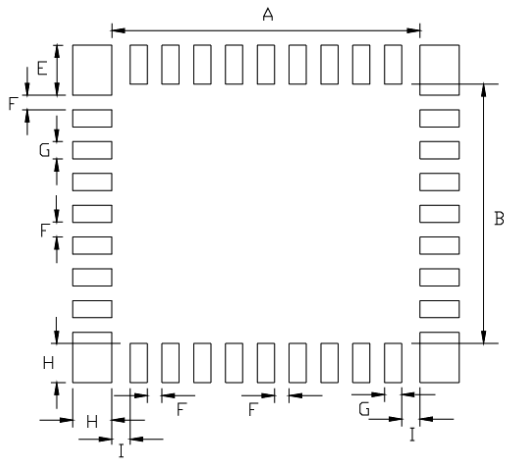
PIN Name	No	I/O	Description
VDD_3.3V	1	I	3.3V for RF circuit
VREG_IN	2	I	Supply 3.3V voltage
VDD_1.8V	3	I/O	Supply 1.8V voltage
PIO1	4	I/O	Programmable Input/Output Line
PIO0	5	I/O	Programmable Input/Output Line
PIO10	6	I/O	Programmable Input/Output Line
AUX_DAC	7	O	Voltage DAC
GND	8	I	Ground
ANT	9	I/O	RF input/output
GND	10	I	Ground
PIO9	11	I/O	Programmable Input/Output Line
PIO2	12	I/O	Programmable Input/Output Line

PIO3	13	I/O	Programmable Input/Output Line
SPI_MOSI	14	I	Serial Peripheral Interface data input
SPI_MISO	15	O	Serial Peripheral Interface data output
SPI_CLK	16	I	Serial Peripheral Interface clock
SPI_CSB	17	I	Chip select for Serial Peripheral Interface data, active low
GND	18	I	Ground
RESET	19	I	Reset, active low
PIO5	20	I/O	Programmable Input/Output Line
PIO4	21	I/O	Programmable Input/Output Line
USB_DP	22	I/O	USB data+ with selectable internal 1.5kohm pull-up resistor
USB_DN	23	I/O	USB Data-
PCM_IN	24	I	Synchronous data input
PCM_CLK	25	I/O	Synchronous data clock
PCM_SYNC	26	I/O	Synchronous data sync
PCM_OUT	27	O	Synchronous data output
GND	28	I	Ground
UART_RTS	29	O	UART request to send active low
UART_TX	30	O	UART data output active high
UART_CTS	31	I	UART clear to send active low
UART_RX	32	I	UART data input active high
AIO0	33	I/O	Analogue Programmable Input/Output
XTAL_OUT	34	O	Drive for crystal
XTAL_IN	35	I	For crystal or external clock input
GND	36	I	Ground

6.3 EEPROM parameter setting

- Mac Address inquired before delivery
- Download through SPI interface
- 6 pins (pin pitch >1.27mm)
- Sequence: **GND**(pin 18), **3.3V**(pin 1), **SPI_CSB**(pin 17), **SPI_MOSI**(pin 14), **SPI_CLK**(pin 16), **SPI_MISO**(pin 15)

6.4 Layout Guide

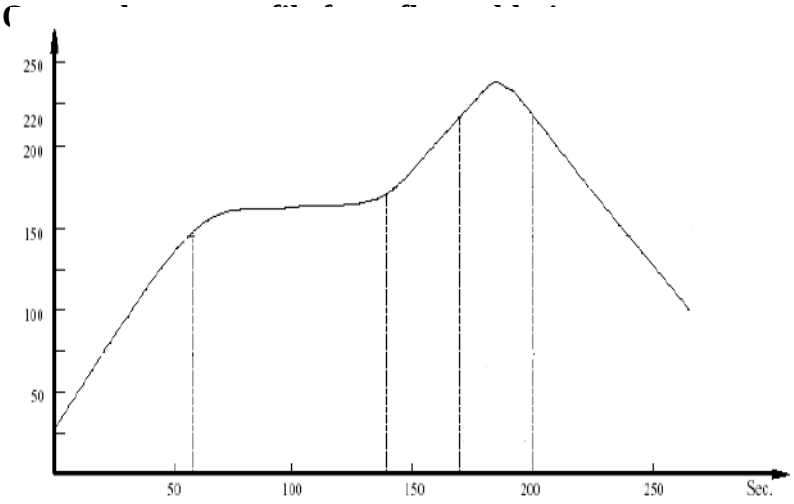


A	6.3 ± 0.1mm	E	1.025 ± 0.05mm	G	0.35 ± 0.05mm
B	5.3 ± 0.1mm	F	0.3 ± 0.05mm		
H	0.8 ± 0.1mm	I	0.375 ± 0.05mm		

6.5 Re-flow Temperature-Time Profile

The data here is given only for guidance on solder and has to be adopted to your process and other re-flow parameters for example the used solder paste. The paste manufacturer provides a re-flow profile recommendation for his product.

C

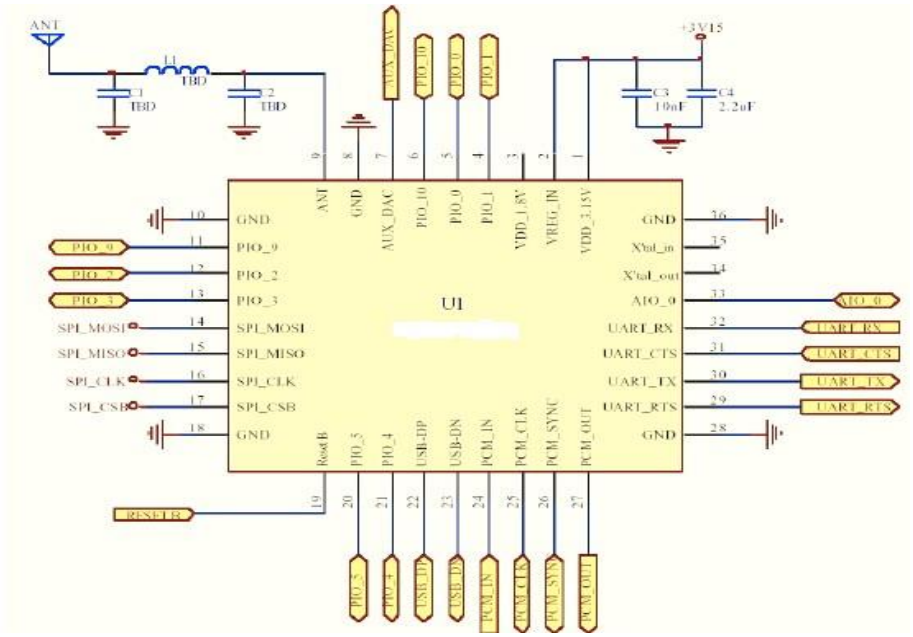


Time [s]

Opposite side re-flow is prohibited due to module weight.

Devices will withstand the specified profile and will withstand up to 2 re-flows to a maximum temperature of 260°C.

6.6 Application schematic



7. Package

Tray Type :

Quantity : 260pcs/tray

Small Box : (L)323 *(W)136 *(H)6.5 (mm)

Add：10F,NO.510,SEC.5,CHUNG HSIAO E. RD, TAIPEI, TAIWAN

Tel：886-2-2346-2323 Fax：886-2-2346-3939

E-mail：spk@spkecl.com WEB:http://www.spkecl.com