SPK Bluetooth 4.0 Dual Mode BR/EDR/LE UART HCI module datasheet

Doc. Version : 20140207


Product ID	**EBMA19A** **EBMA19B**
Product Name	**Bluetooth 4.0 Dual Mode BR/EDR/LE UART HCI module**
Firmware Version	
Hardware Version	**Rev.1.0.2**

1. DESCRIPTION

Dual mode means it supports classic Bluetooth basic rate (BR) and enhanced data rate (EDR) operations as well as the new low energy (LE) standard.

EBMA19 is CSR single-chip radio and baseband IC solution for Bluetooth 2.4GHz systems including EDR to 3Mbits/s and Bluetooth low energy. BLE allows mobile devices to exchange simple data sets with very low consumption. Example use cases include watches, medical sensors and fitness trainers that can operate for many years from a small coin cell battery.

2. FEATURES

- Bluetooth Low Energy available with CSR8811WLCSP
- Bluetooth v4.0 specification
- Dual-mode Bluetooth®/Bluetooth low energy radio
- Can form part of Bluetooth v4.0 + HS system
- Class 1 or Class 2 Bluetooth power levels
- High-sensitivity Bluetooth and Bluetooth low energy receiver
- Full-speed Bluetooth operation with full piconet and scatternet support
- On-chip balun and minimal BOM
- Low-power selectable 1.2 to 3.6V I/O
- Integrated I/O and core regulators
- High-speed UART port (up to 4Mbps)
- Two PCM/I²S digital audio interfaces
- Support for IEEE 802.11 coexistence
- Dimensions: 14.5mm x 7.125mm x 1.8mm(EBMA19)

14.5mm x 12mm x 2.5mm(EBMA19, with printed antenna)

■ Storage temperature range: -40ºC ~ +85ºC
■ Operating temperature range: -30ºC ~ +85ºC

3. APPLICATIONS

■ Low-cost phones
■ Feature phones
■ Smart phones
■ The high-power Class 1 Bluetooth transmitter removes the requirement for external amplification.
■ The balun is integrated, which results in a single ended 50Ω port that does not require additional matching components.
■ Integrated LDOs, with minimum decoupling components, allow the chip to be operated directly from the battery or a regulated supply.
■ To improve the performance of both Bluetooth and IEEE 802.11b/g/n co-located systems a wide range of coexistence features are supported.

3.1 Device Details

3.1.1 Bluetooth low energy

■ Dual mode Bluetooth low energy radio
■ Supports simultaneous Bluetooth BR/EDR and multiple low energy connections
■ Support for on-chip AES encryption
■ Adaptive Bluetooth/Bluetooth low energy scheduler
■ On-chip whitelist support

3.1.2 Bluetooth Radio

■ On-chip balun (50Ω impedance in TX and RX modes)
■ No external trimming is required in production
■ Bluetooth v4.0 specification compliant

3.1.3 Bluetooth Transmitter

■ Class 1 and Class 2 support without need for external power amplifier or TX/RX switch
■ DQPSK and 8DPSK

3.1.4 Bluetooth Receiver

■ Integrated channel filters
■ Digital demodulator for improved sensitivity and cochannel rejection
■ Real time digitised RSSI available on HCI interface

■ Fast AGC for enhanced dynamic range
■ Channel classification for AFH
■ DQPSK and 8DPSK

3.1.5 Baseband and Software

■ Internal RAM allows full-speed data transfer, mixed voice and data, and full piconet operation, including all medium rate packet types
■ Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping. Includes support for eSCO and AFH
■ Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air

3.1.6 Bluetooth Stack

■ Bluetooth Protocol Stack runs on the on-chip MCU in the configuration Standard HCI over UART

3.1.7 Synthesiser

■ Fully integrated synthesiser requires no external VCO varactor diode, resonator or loop filter
■ Compatible with external clock 19.2MHz to 40MHz
■ Can be operated from external crystal

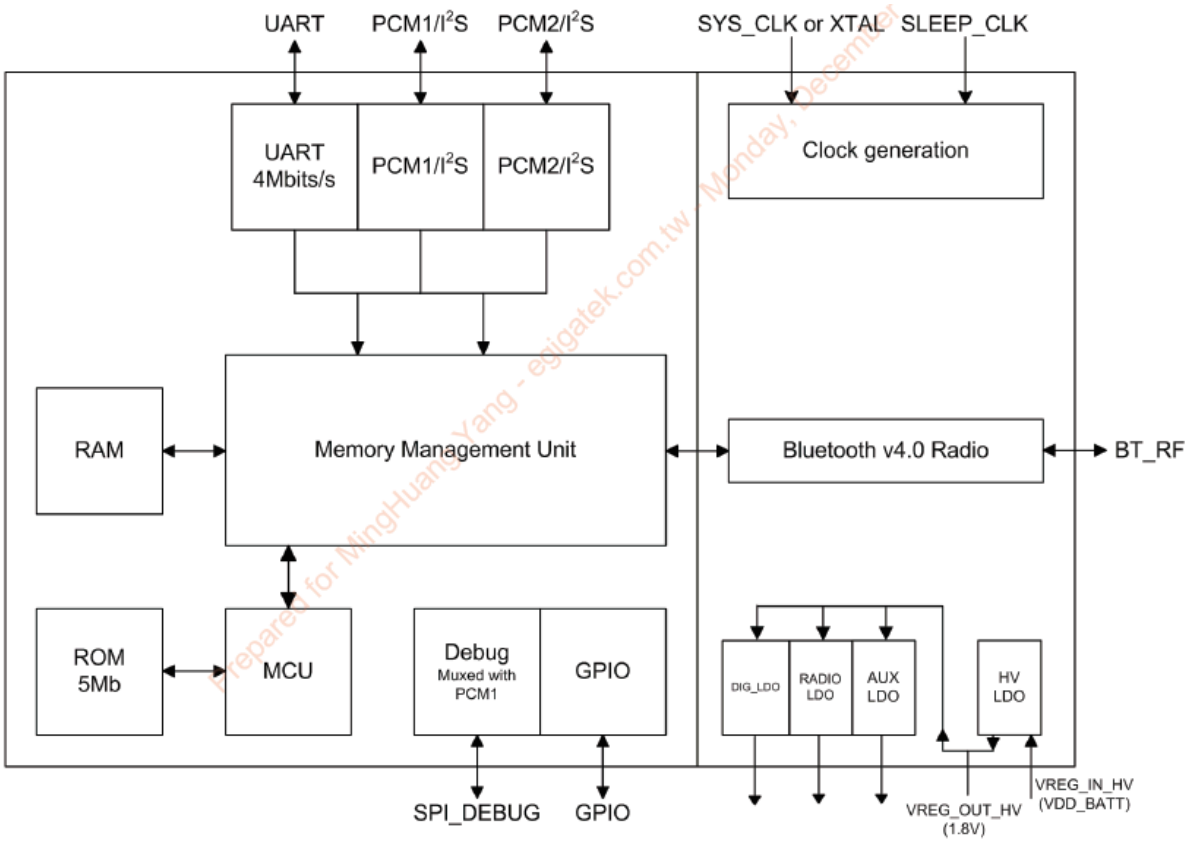
3.1.8 Physical Interfaces

■ UART interface with programmable baud rate up to 4Mbits/s
■ BCSP, H4, H4DS and H5 support
■ 2 PCM/I2S interfaces
■ Synchronous serial interface up to 4Mbits/s for system debugging

3.1.9 Auxiliary Features

■ Power management includes digital shutdown, and wake up commands with an integrated low power oscillator for ultra low power Park/Sniff/Hold mode
■ Auto Baud Rate setting, depending on host interface
■ On-chip linear regulators:
  ■ 1.8V output from typical 2.5 to 4.8V (5.5V for short periods) input (load current 100mA)
  ■ Low dropout linear regulators producing internal supply voltages from 1.8V, and allowing operation directly from a battery
■ Power-on-reset cell detects low supply voltage
■ Arbitrary sequencing of power supplies is permitted

4. BLOCK DIAGRAM



5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Rating	Min	Max
Storage temperature	-40□	+85□
VBAT operation(a)	2.3V	4.8V
Low-voltage operation (bypassing high-voltage linear regulator)	1.7V	2.0V
I/O supply voltage	-0.4V	3.6V
Other terminal voltages	VSS-0.4	VDD+0.4

(a) Short-term operation up to a maximum of 10% of product lifetime is permissible without damage, but output regulation and other specifications are not guaranteed in excess of 4.8V.

5.2 Recommended Operating Conditions

Operating Condition	Min	Max
Operating temperature range	-30□	85□
VBAT operation	2.3V	4.8V
Low-voltage operation (bypassing high-voltage linear regulator	1.75V	1.95V
I/O supply voltage (VDD_HOST and VDD_PADS)	1.2	3.6V
VREG_EN_RST#	VSS_PADS	VDD_HOST

5.3 Input/Output Terminal Characteristics

5.3.1 High-voltage Linear Regulator

Switch-mode Regulator	Min	Typ	Max	Unit
Input voltage	2.3	3.3	4.8	V
Output voltage	1.75	1.85	1.95	V
Temperature coefficient	-200	-	200	ppm/°C
Output noise, frequency range 100Hz to 100kHz	-	-	0.4	mV rms
Settling time, settling to within 10% of final value	-	-	5	µs
Output current	-	-	100	mA
Quiescent current (excluding load, I_{load} < 1mA)	30	40	60	µA
Low-power Mode				
Quiescent current (excluding load, I_{load} < 100mA)	14	18	23	µA

5.3.2 Low-voltage VDD_DIG Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Output voltage	0.90	-	1.25	V
Output current	-	-	30	mA

5.3.3 Low-voltage VDD_AUX Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Output voltage	1.30	1.35	1.40	V
Output current	-	-	5	mA

5.3.4 Low-voltage VDD_RADIO Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Output voltage	1.30	1.35	1.45	V
Output current	-	-	60	mA

5.3.5 Digital

Digital Terminals	Min	Typ	Max	Unit
Input Voltage				
V_{IL} input logic level low	-0.4	-	0.4	V
V_{IH} input logic level high	0.7 x VDD	-	VDD+0.4	V
Output Voltage				
V_{OL} output logic level low, I_{OL} = 4.0mA	-	-	0.4	V
V_{OH} output logic level high, I_{OH} = -4.0mA	0.75 x VDD	-	-	V
Input and Tristate Currents				
Strong pull-up	-150	-40	-10	µA
Strong pull-down	10	40	150	µA
Weak pull-up	-5.0	-1.0	-0.33	µA
Weak pull-down	0.33	1.0	5.0	µA
C_I input capacitance	1.0	-	5.0	pF

6. HOST INTERFACE

Use the host interface to:

- Configure EBMA19 to suit the target platform requirements.
- Transfer data to and from other Bluetooth devices.

6.1 UART Interface

This is a standard UART interface for communicating with other serial devices. EBMA19 UART interface provides a simple mechanism for communicating with other serial devices using the RS-232 protocol.

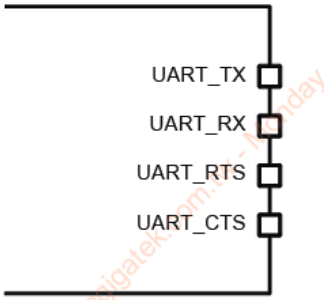


Figure 6.1: Universal Asynchronous Receiver Transmitter(UART)

Figure 6.1 shows the 4 signals that implement the UART function. When EBMA19 is connected to another digital device, UART_RX and UART_TX transfer data between the 2 devices. The remaining 2 signals, UART_CTS and UART_RTS, implement RS232 hardware flow control where both are active low indicators.
If UART_CTS and UART_RTS are not required for hardware flow control, they are reconfigurable as PIO. UART configuration parameters, such as baud rate and packet format, are set using EBMA19 firmware.
Note:To communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

Parameter		Possible Values
Baud rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4Mbaud (≤1%Error)
Flow control		RTS/CTS or None
Parity		None, Odd or Even
Number of stop bits		1 or 2
Bits per byte		8

Table 6.1: Possible UART Settings

The UART interface resets EBMA19 on reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as Figure 6.2 shows. If tBRK is longer than the value, defined by the PSKEY_HOSTIO_UART_RESET_TIMEOUT, a reset occurs. This feature enables a host to initialise the system to a known state. Also, EBMA19 can issue a break character for waking the host.

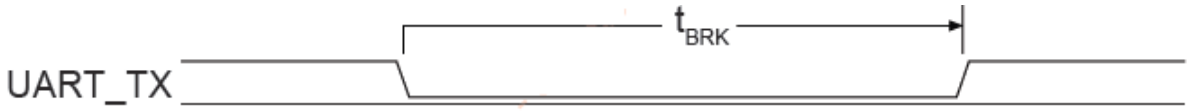


Figure 6.2: Break Signal

Refer to PSKEY_UART_BITRATE for more information about the baud rates and their values.

Generated baud rate is independent of selected incoming clock frequency.

6.1.1 UART Configuration While Reset is Active

The UART interface for EBMA19 is tri-state while the chip is being held in reset. This enables the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tri-state when EBMA19 reset is de-asserted and the firmware begins to run.

7 AUDIO INTERFACES

EBMA19 has two digital audio interfaces that are configurable as either PCM or I² S ports.

7.1 PCM Interface

There are two audio interfaces. Each can be independently configured as an I2S or a PCM port. The PCM1 interface
also shares the same physical set of pins with the SPI interface as described in the Device Terminal Functions section. Either interface is selected using SPI_PCM#_SEL:

■ SPI_PCM#_SEL = 1 selects SPI
■ SPI_PCM#_SEL = 0 selects PCM

Important Note:
The PCM description refers to both PCM1 or PCM2.
The audio PCM interface on the CSR8811 supports:

■ Continuous transmission and reception of PCM encoded audio data over Bluetooth.
■ Processor overhead reduction through hardware support for continual transmission and reception of PCM data
■ A bidirectional digital audio interface that routes directly into the baseband layer of the firmware. It does not pass through the HCI protocol layer.
■ Hardware on the CSR8811 for sending data to and from a SCO connection.
■ Up to 3 SCO connections on the PCM interface at any one time.
■ PCM interface master, generating PCM_SYNC and PCM_CLK.
■ PCM interface slave, accepting externally generated PCM_SYNC and PCM_CLK.
■ Various clock formats including:
■ Long Frame Sync
■ Short Frame Sync
■ GCI timing environments
■ 13-bit or 16-bit linear, 8-bit μ-law or A-law companded sample formats.
■ Receives and transmits on any selection of 3 of the first 4 slots following PCM_SYNC.

The PCM configuration options are enabled by setting the PS Key PSKEY_PCM_CONFIG32.

7.1.1 PCM Interface Master/Slave

When configured as the master of the PCM interface, CSR8811 generates PCM_CLK and PCM_SYNC.

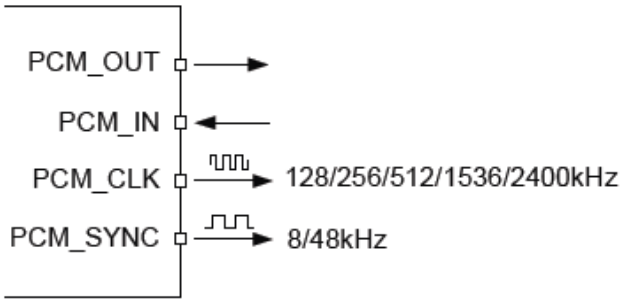


Figure 7.1: PCM Interface Master

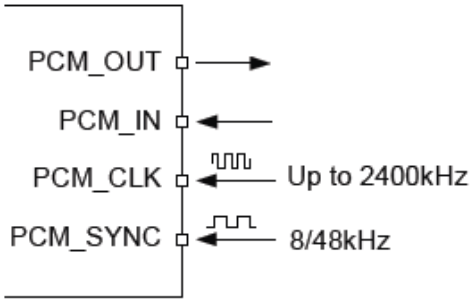


Figure 7.2: PCM Interface Slave

8. PIN DESCRIPTION

8.1 Pin Numbering

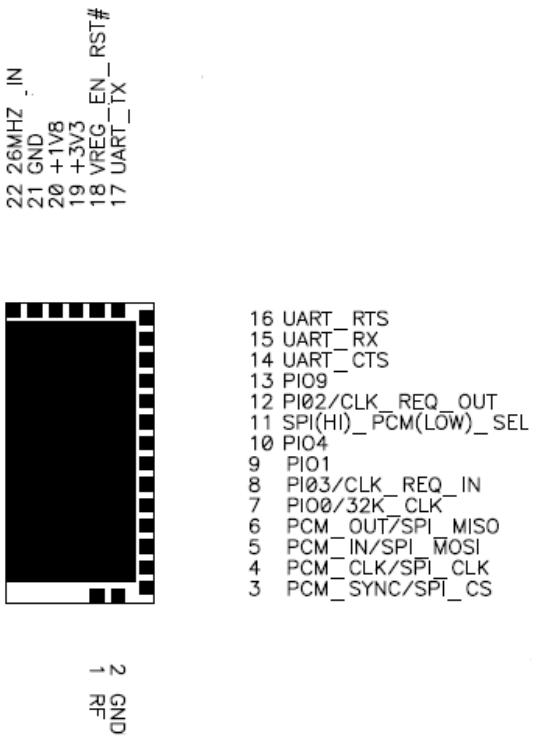


Figure 8.1 EBMA19A Pin Numbering

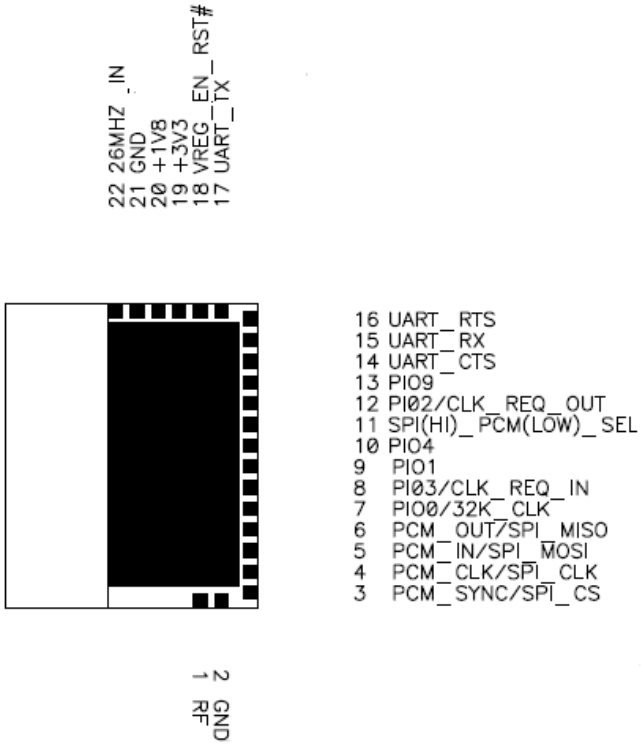


Figure 8.2 EBMA19B Pin Numbering

8.2 Pin Definition

PIN Name	No		Description
RF	1		Bluetooth transmitter/receiver
GND	2		Ground
PCM_SYNC/SPI_CS	3		PCM synchronous data sync/ SPI SPI chip select, active low
PCM_CLK/SPI_CLK	4		PCM synchronous data clock/ SPI clock
PCM_IN/SPI_MOSI	5		PCM synchronous data input/ SPI data input
PCM_OUT/SPI_MISO	6		PCM synchronous data output/ SPI data output
PIO0/32K_CLK	7		Programmable input/output line and 32kHz sleep clock input
PIO3/CLK_REQ_IN	8		Programmable input/output line, clock REQ in
PIO1	9		Programmable input/output line
PIO4	10		Programmable input/output line
SPI(HI)_PCM(LOW)_SEL	11		Control line to select SPI or PCM interface, high=SPI, low=PCM

PIO2	12		Programmable input/output line, clock REQ out
PIO9	13		Programmable input/output line
UART_CTS	14		UART clear to send, active low
UART_RX	15		UART data input, active high
UART_RTS	16		UART request to send, active low
UART_TX	17		UART data output, active high
VREG_EN_RST#	18		Take high to enable internal regulators. Also acts as active low reset
+3V3	19		3V3 supply Voltage
+1V8	20		1V8 supply Voltage
GND	21		Ground
26MHZ_IN	22		For external system crystal input

9. MECHANICAL CHARACTERICS

9.1 Dimensions

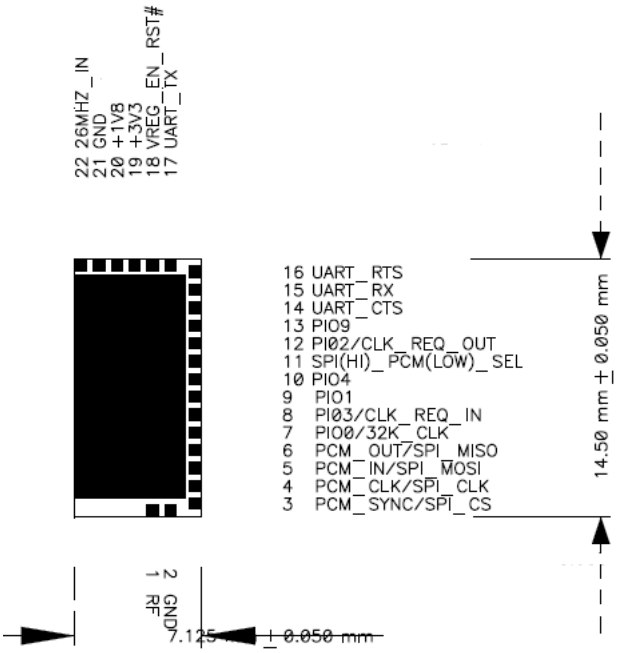


Figure 9.1 EBMA19A dimension

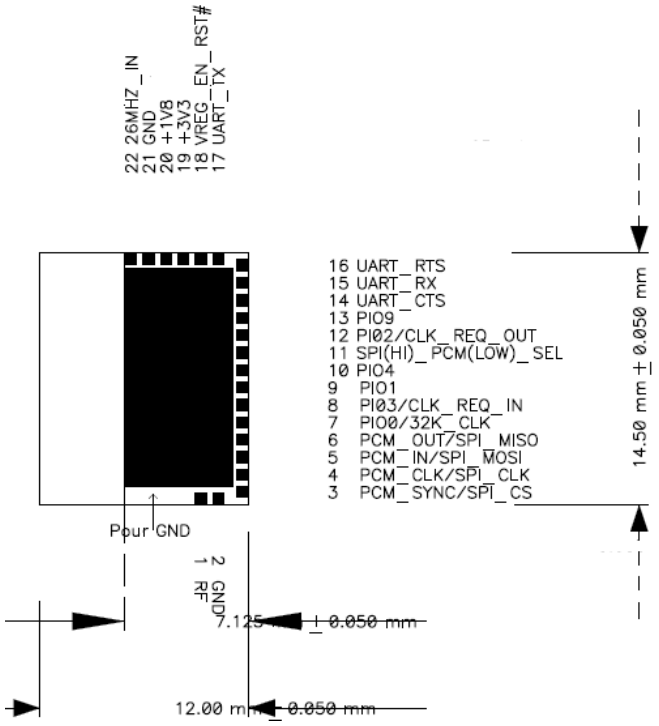


Figure 9.2 EBMA19B dimension

9.2 Recommended Land Pattern

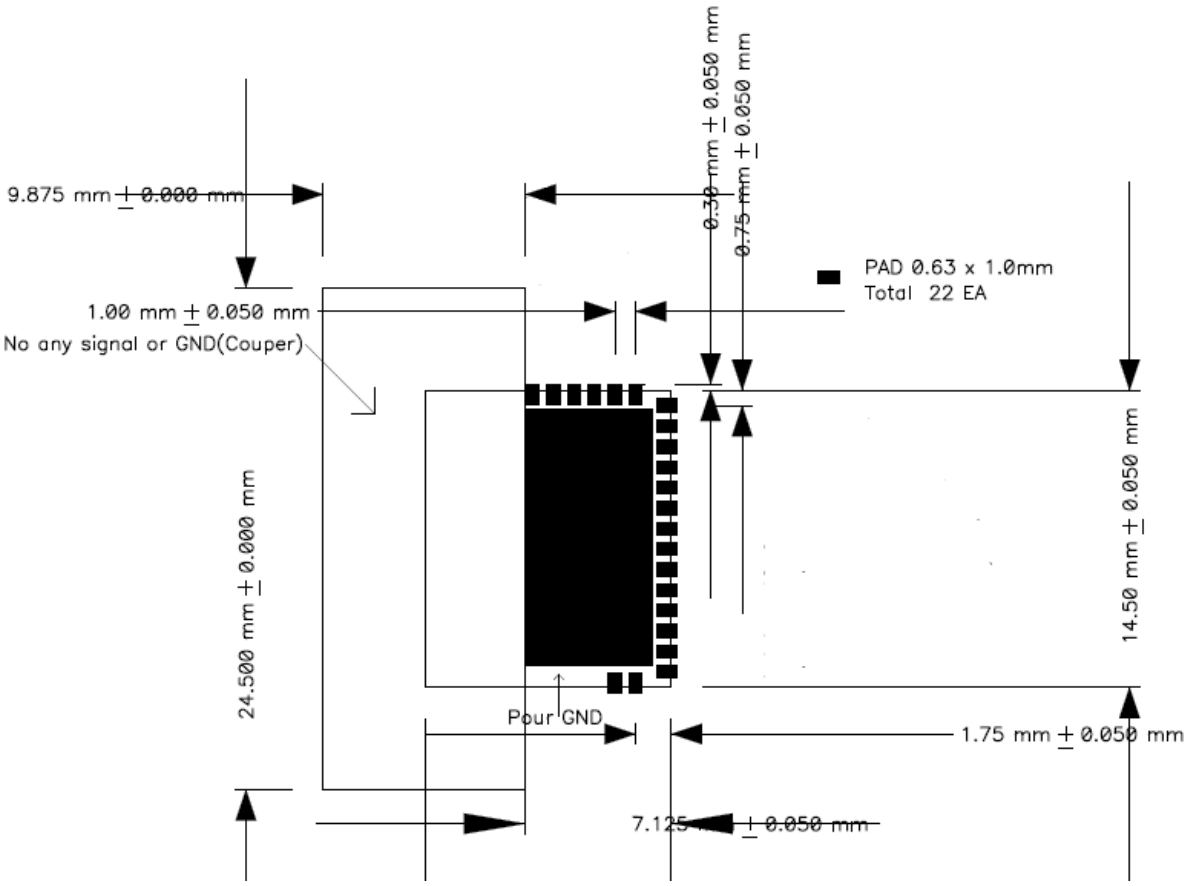
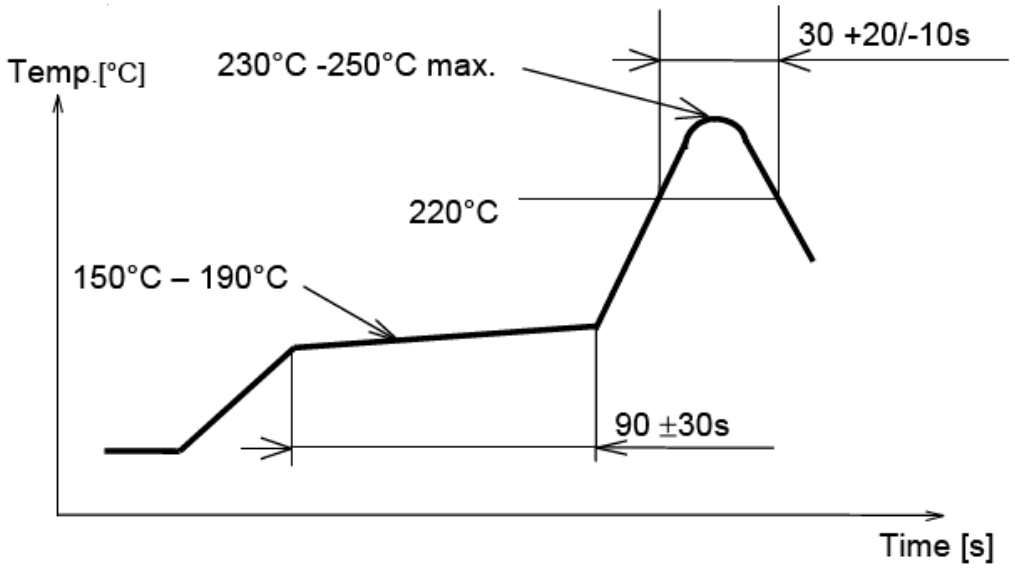


Figure 9.4 EBMA19A and EBMA19B land pattern

9.3 Typical Solder Reflow Profile

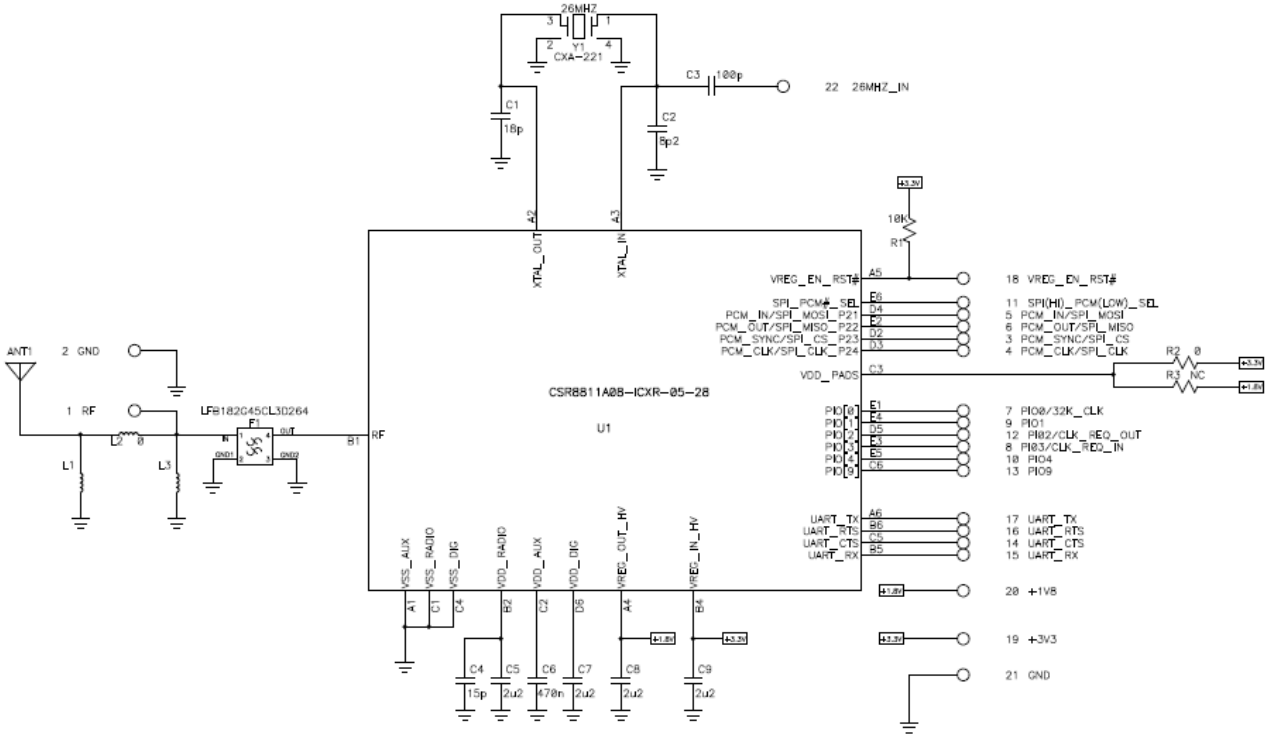


9.4 Housing Guidelines

The individual case must be checked to decide whether a specific housing is suitable for the use of the internal antenna. A plastic housing must at least fulfill the following requirements:

- ✧ Non-conductive material, non-RF-blocking plastics
- ✧ No metallic coating
- ✧ ABS is suggested

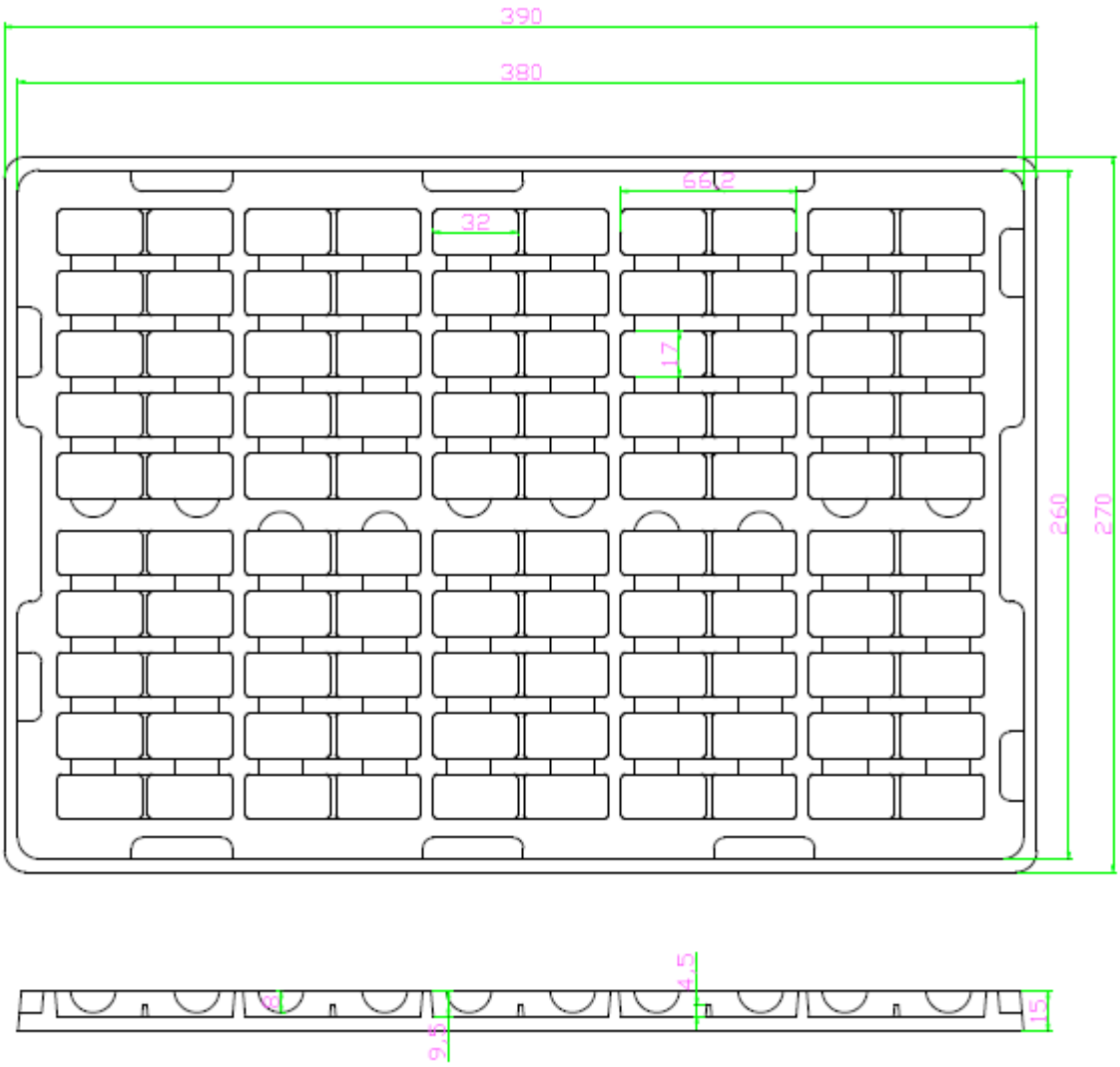
9.5 Application schematic



10. PACKAGE

Tray Type

a. **Carrier not be exceed 1mm in 100mm.**
b. **Packing dimensions meet : 390mm * 270mm * 15mm**
c. **Material : white anti-static polystyrene**
d. **Component load per tray : 100pcs**



SPK Bluetooth module design data